Operating Guide

SN’s Digital I/O Function

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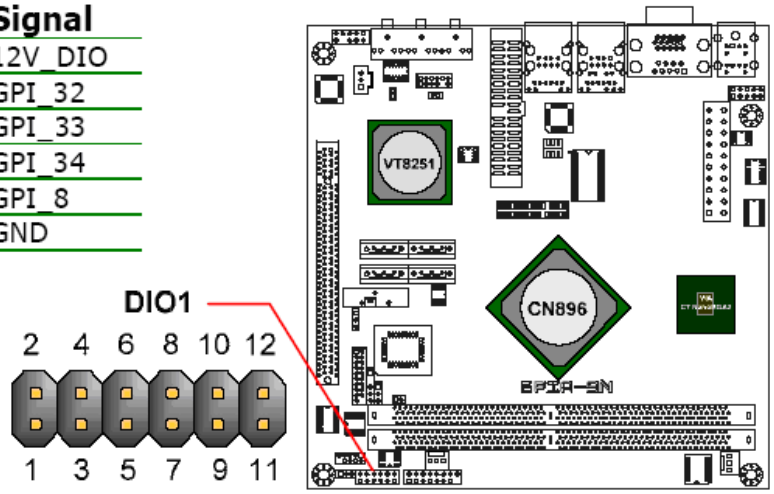
Digital I/O (DIO 1: 4 GPI, 4 GPO) Introduction

Digital I/O Connector: DIO1

General purpose input and output for POS systems.

Pin	Signal	Pin	Signal
1	5V_DIO	2	12V_DIO
3	GPO_1	4	GPI_32
5	GPO_4	6	GPI_33
7	GPO_6	8	GPI_34
9	GPO_7	10	GPI_8
11	GND	12	GND



VT8251 GPI/O Control Porting Table

Signal Name	Pin No.	Signal Select Register	Signal Description
GPI32	P3		input value on PMIO_RX47[0]
GPI33	P2		input value on PMIO_RX47[1]
GPI34	R3		input value on PMIO_RX47[2]
GPI8	D26	PMU_RXE4[3]	PMU_RXE4[3] = 0: GPI8, GPI8 input value on PMIO_RX49[0]
GPO1	AD3		GPO1 output control on PMIO_RX4C[1]
GPO4	AA3	PMU_RX95[1]	PMU_RX95[1] = 1: GPO4 GPO4 output control on PMIO_RX4C[4]
GPO6	AF2	PMU_RXE4[1]	PMU_RXE4[1] = 1: GPO6 GPO6 output control on PMIO_RX4C[6]
GPO7	N3	PMU_RXE4[2]	PMU_RXE4[2] = 0: GPO7 GPO7 output control on PMIO_RX4C[7]

VT8251 Power Management I/O Base – Offset 8B-88

31 - 16 Reserved……always reads 0

15 - 7 Power Management I/O Register Base Address

Port Address for the base of the 128-byte Power Management I/O Register Block, corresponding to AD[15:7]. See "Power Management I/O Space Registers" in data sheet of VT8251 for definitions of the registers in the Power Management I/O Register Block.

6 - 0 0000001b

Digital Output Programming

Programming Construction:

Step1: Get PMIO Base Address

Step2: Enable GPI/GPO

Step3: Write GPO7 output

Program Example:

```
#define      VT8251     0x80008800
WORD wPmioBase;
/*************************************************************************/
/* inp(): IN data from I/O port by byte                                  */
/* inpd(): IN data from I/O port by double word                          */
/* outp(): OUT data to I/O port by byte                                  */
/* outpd(): OUT data to I/O port by double word                          */
/*************************************************************************/
/*************************************************************************/
/* GetPMIOBaseAddr                                                       */
/*************************************************************************/
```

```
GetPMIOBaseAddr()
{
 DWORD          pciAddr;
 /*
  * For (VT8251)
  * PMIO Base Address is located in PCI configuration space
  * Bus 0, device 17, function 0, offset 0x88
 */
 pciAddr    = VT8251 | 0x88;
 outpd(0x0CF8, pciAddr);
 wPmioBase = inpd(0x0CFC);
 wPmioBase &= 0xFFFE;
 printf("PMIO Base address = %x\n", wPmioBase);
} /* end GetPMIOBaseAddr */
/*****************************************************************************
 * Enable and initialize GPO port (eg. Enable GPO 7)
 *****************************************************************************/
GPOEnable()
{
 DWORD          pciAddr;
 DWORD          value;
 /*
  * For (VT8251)
  * GPO Control is located in PCI configuration space
  * Bus 0, device 17, function 0, offset 0xE4
 */
 pciAddr    = VT8251 | 0xE4;
 outpd(0x0CF8, pciAddr);
 value = inpd(0x0CFC);
 /*
  * eg. Enable GPO 7
  * GPO 7:    RxE4[2] = 0
 */
 value |= 0x00000000;                /* set 0 to bit 2 */
 outpd(0x0CFC, value);
} /* end GPOEnable */
/*****************************************************************************
 * Put byte to GPO (eg. Pull high GPO 7)
 *****************************************************************************/
```

```
GPOSet()
{
  BYTE              data;
  /*
    * GPO 7 is in the offset 0x4C bit 7
  */
  data = inp(wPmioBase + 0x4C);
  data |= 0x80;
  /*
    * Out the value to the GPO io address
  */
  outp(wPmioBase + 0x4C, data);
} /* end GPOSet */
```