GC05A2 COB

1/5" 5Mega CMOS Image Sensor

DataSheet

V1.1

2023-02-02

Ordering Information

◆ **GC05A2-WC1XA**

(Colored, 200um, back grinding, reconstructed wafer)

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	AUTHOR(S)
V1.0	2022-12-21	Initial Release	Alisa_miao
V1.1	2023-02-02	Update: 1.Table2-1&Table2-4&Table2-5&Table7-1&Table5-2&Table5-3 2.Figure3-1&Figure3-3&Figure5-3&Figure5-4	Alisa_miao

Galaxycore Incorporation

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Expression	Description
CRA	Chief Ray Angle
MIPI	Mobile Industry Processor Interface
OTP	One Time Programmable Read Only Memory
ADC	Analog-Digital Converter
DD	Dead Pixel & Defect Correction
Digital Input & Output Voltage	for INCLK,SBDA,SBCL,XSHUTDOWN,FSYNC,IDSEL
Test Temperature	Temperature in which image quality test is operated

1. Sensor Overview

1.1 General Description

GC05A2 is a high quality 5Mega Bayer pattern CMOS Image Sensor (CIS) for cellular phone camera application and other products with embedded camera like tablet PC, smart watch, etc. GC05A2 is designed for full-size capturing at 30 frames per second (fps).

The total active pixel array size is 2592x 1944 to meet with the 1/5-inch optical format.

GC05A2 has on-chip 10-bit ADC arrays and corresponding image signal process functions like static DD, black level calibration, etc.

GC05A2 is suitable for fast yet low power consumption application with power supply of AVDD(2.8V)/IOVDD(1.8V or 1.2V)/DVDD(1.2V), which is useful in extending the battery life of cell phones, tablet PCs and a variety of other mobile products.

The CIS provides RAW10 data format through MIPI interface and can be controlled through camera control interface (CCI).

1.2 Block Diagram
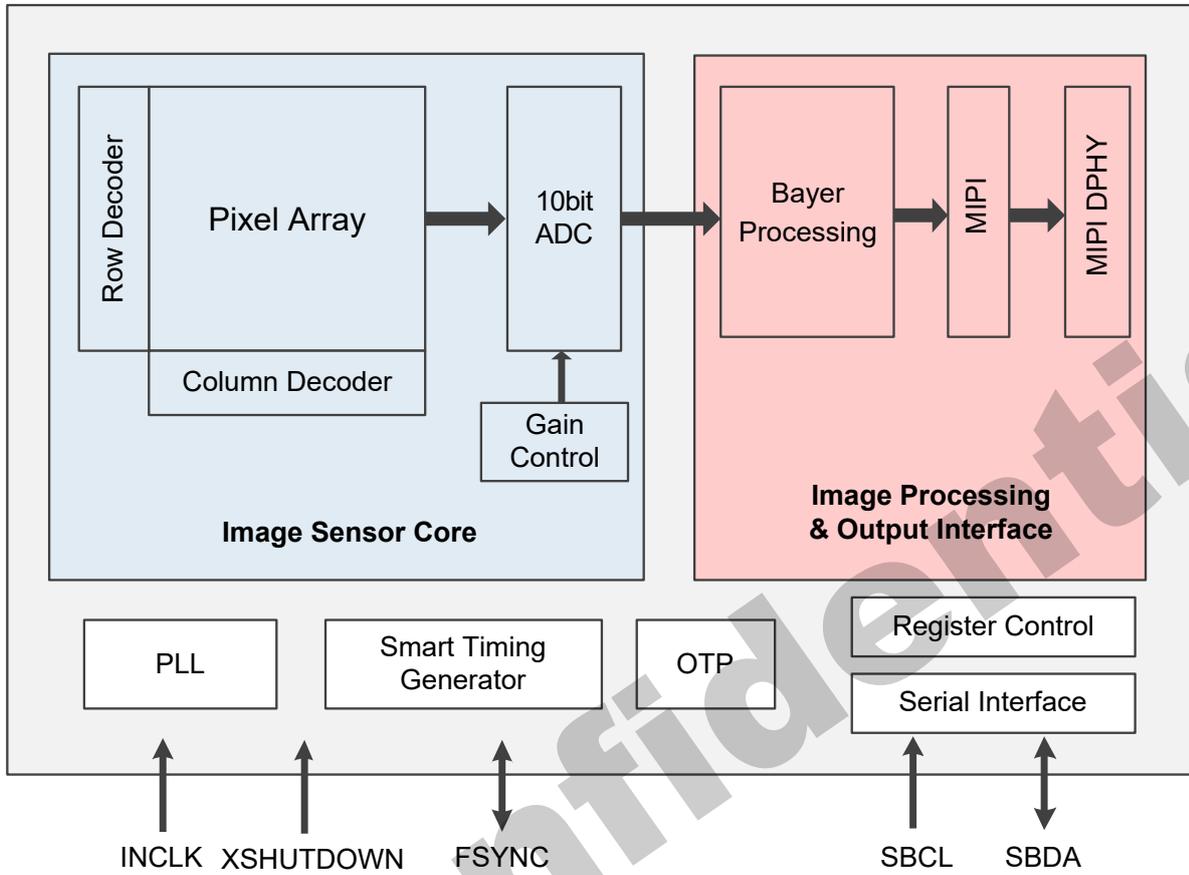
Figure 1-1 Block Diagram

1.3 Features

- Optical format : 1/5 inch
- Pixel size : 1.12μm x 1.12μm BSI
- Active image size : 2592 x 1944
- Color filter : Bayer Pattern
- Output formats : Raw 10bit
- Shutter type : Electronic rolling shutter
- Frame rate : 30fps @ Full size

  : 30fps @1080P (crop)

  : 60fps @ HD (binning)

- MIPI data rate (max) : 1Gbps/lane
- Lane number : 2-lane
- ADC Accuracy : 10 bits
- Power supply requirement : 2.70~3.00V for AVDD (Typical 2.80V)

  1.15~1.30V for DVDD (Typical 1.20V)

  1.15~1.25V / 1.70~1.90V for IOVDD

  (Typical 1.20V / 1.80V)

- Image Flip : Horizontal/Vertical mirror
- Operation temperature : -20℃ ~ 70℃
- Analog Gain : Max. 16x
- OTP support : 64K bits(56K bits for customer)
- Package : COB/CSP/COM
- Max. optical lens CRA : 31.9°
- PLL support
- Windowing support
- Dual sync application support (master/slave)

2. Electrical Characteristics

2.1 Absolute Maximum Rating

Table 2-1 Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit	Note
Analog power supply	V_{AVDD_MAX}	-0.3	-	3.9	V	Refer to GND level
Digital power supply	V_{DVDD_MAX}	-0.3	-	1.8	V	
I/O power supply	V_{IOVDD_MAX}	-0.3	-	3.6	V	
Digital input voltage	V_{I_MAX}	-0.3	-	V_{IOVDD}+0.3	V	
Digital output voltage	V_{O_MAX}	-0.3	-	V_{IOVDD}+0.3	V	
Storage temperature	T_{STR}	-40	-	85	℃	

2.2 Operating Conditions

Table 2-2 Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Analog power supply	V_{AVDD}	2.7	2.8	3.0	V
Digital power supply	V_{DVDD}	1.15	1.2	1.3	V
I/O power supply	V_{IOVDD}	1.7/1.15	1.8/1.2	1.9/1.25	V
Digital input voltage	V_I	0	-	V_{IOVDD}	V
Digital output voltage	V_O	0	-	V_{IOVDD}	V
Test temperature	T_{TEST}	21	25	27	℃
Operating temperature	T_{OPR}	-20	-	70	℃
Performance temperature	T_{SEPC}	0	-	60	℃

2.3 DC Characteristics

Table 2-3 DC Characteristics

Items	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	-	$0.7 \times V_{IOVDD}$	-	-	V
	V_{IL}	-	-	-	$0.3 \times V_{IOVDD}$	V
Input leakage current	I_{IL}	$V_{IN} = V_{IOVDD}$ or VSS	-10	-	10	µA
High level output voltage	V_{OH}	$I_{OH} = -100µA$	$0.7 \times V_{IOVDD}$	-	-	V
Low level output voltage	V_{OL}	$I_{OL} = 100µA$	-	-	$0.3 \times V_{IOVDD}$	V
High-z output leakage current	I_{OZ}	$V_{OUT} = V_{DVDD}$ or VSS	-10	-	10	µA

Note:

1. High-z output is applied to SBDA, SBCL & MIPI pins when in High-z state.

2.4 Input Clock Square Waveform Specifications
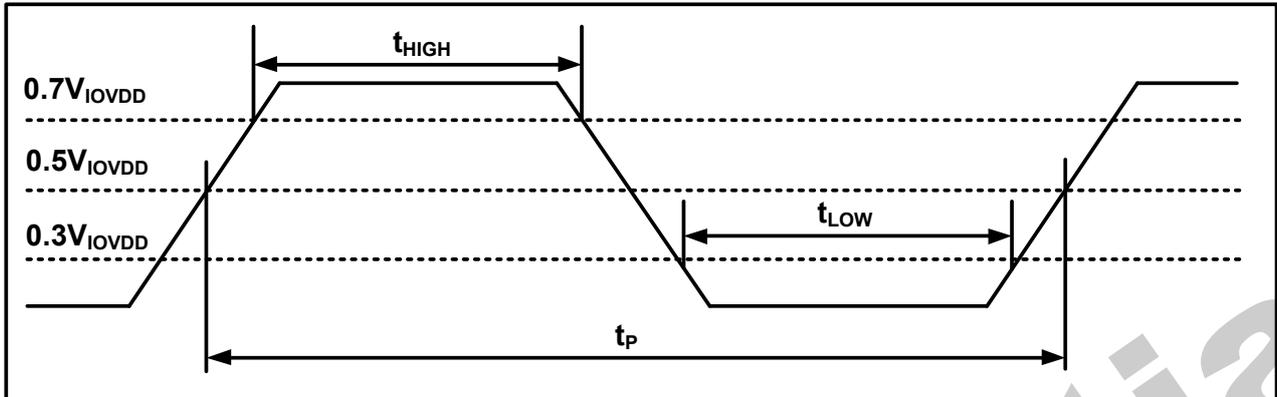
Figure 2-1 INCLK Wave Diagram

INCLK is the input clock to sensor. Table 2-4 shows some detailed parameters of INCLK square waveform specifications.

Table 2-4 INCLK Square Waveform Specifications

Item	Symbol	Min.	Typ.	Max	Unit
INCLK Frequency	f_{INCLK}	12	24	27	MHz
INCLK jitter (period, peak-to-peak)	T_{jitter}			600	ps
INCLK high level width	T_{HIGH}	0.4tp		0.6tp	ns
INCLK low level width	T_{LOW}	0.4tp		0.6tp	ns
INCLK period	tp	37.0		83.3	ns
INCLK duty cycle	R_{DUTY}	40		60	%

2.5 Power Consumption

Table 2-5 Power Consumption

Item	Symbol	Min	Typ	Max	Unit
2592x1944 @30fps	I_{AVDD}	-	15.5	25	mA
	I_{DVDD}	-	40	60	mA
	I_{IOVDD}	-	2.8	5	mA
1296x972 @30fps	I_{AVDD}	-	15.5	25	mA
	I_{DVDD}	-	30	50	mA
	I_{IOVDD}	-	2.8	5	mA
720p @60fps	I_{AVDD}	-	15.5	25	mA
	I_{DVDD}	-	30	50	mA
	I_{IOVDD}	-	2.8	5	mA
1080p @30fps	I_{AVDD}	-	15.5	25	mA
	I_{DVDD}	-	30	50	mA
	I_{IOVDD}	-	2.8	5	mA
Standby current	I_{AVDD}	-	20	100	µA
	I_{DVDD}	-	500	5000	µA
	I_{IOVDD}	-	20	300	µA
Power off current	I_{total}	-		0	µA

Note:

1. All operating current are measured with INCLK running at 24MHz.

2. Standby current is measured with the condition that XSHUTDOWN set Low.

3. We recommend that power should be turned off when lower power consumption is required.

3. Pad Configuration
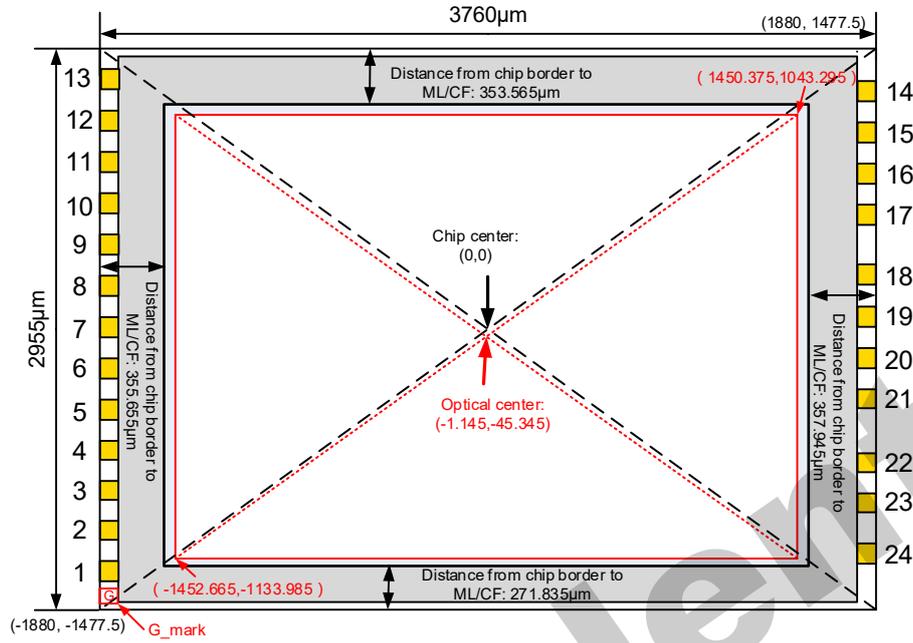
Figure 3-1 Chip Dimension Top View
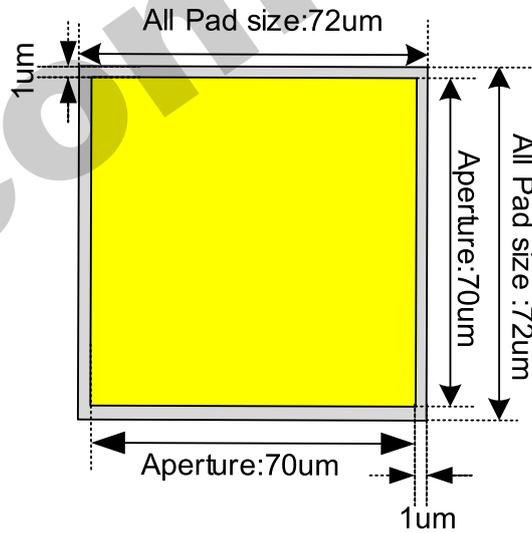
Figure 3-2 Pad Size and Aperture

<div style="text-align:center">GALAXYCORE</div>

<div style="text-align:center">Table 3-1 Pad Configuration</div>

Die size	• Without Scribe Lane: 3760µm x 2955µm • With Scribe Lane: 3840µm x 3035µm
Minimum pad pitch ：	190µm
Bonding pad open size	70 µm x 70 µm
Total number of pads	24ea (w/o dummy PADs)
Total number of bonding pads	24ea
Optical center	(-1.145µm , -45.345µm)

3.1 Pad Description

Pin	X(um)	Y(um)	Name	Type	A/D	Description
1	-1830	-1336.4	DGND	Ground	D	Ground for digital
2	-1830	-1136.9	DVDD12	Power	D	Digital power supply pin:1.15~1.3V
3	-1830	-942.9	VDDIO	Power	D	Power supply for I/O circuits: 1.15~1.25V/1.7~1.9V
4	-1830	-735.9	VOTP	Power	D	OTP power supply pin
5	-1830	-501.9	INCLK	Input	D	Sensor input clock
6	-1830	-291.9	FSYNC	I/O	D	Frame sync control
7	-1830	-84.9	IDSEL	Input	D	I2C ID select
8	-1830	105.1	SBCL	Input	D	Two-wire serial bus, clock
9	-1830	314.1	SBDA	I/O	D	Two-wire serial bus, data
10	-1830	527.1	XSHUTDOWN	Input	D	Reset and PWDN multiplexing: 0: standby state 1: normal operation
11	-1830	772.1	AGND	Ground	A	Ground for analog

Pin	X(um)	Y(um)	Name	Type	A/D	Description
12	-1830	972.1	AVDD28	Power	A	Main power supply pin:2.7~3.0V.
13	-1830	1170.1	VREF	Power	A	Internal power supply
14	1829.95	1169.43	VTX	Power	A	Internal power supply
15	1829.95	979.43	DVDD12	Power	D	Digital power supply pin: 1.15~1.3V
16	1829.95	769.43	DGND	Ground	D	Ground for digital
17	1829.95	579.43	MDN0	Output	D	MIPI data <0> (-)
18	1829.95	269.43	MDP0	Output	D	MIPI data <0> (+)
19	1829.95	79.43	DGND	Ground	D	Ground for MIPI
20	1829.95	-124.57	DVDD12	Power	D	Digital power supply pin: 1.15~1.3V
21	1829.95	-380.57	MCN	Output	D	MIPI clock (-))
22	1829.95	-690.57	MCP	Output	D	MIPI clock (+)
23	1829.95	-880.57	MDN1	Output	D	MIPI data <1> (-)
24	1829.95	-1190.57	MDP1	Output	D	MIPI data <1> (+)

3.2 Peripheral Circuit Design
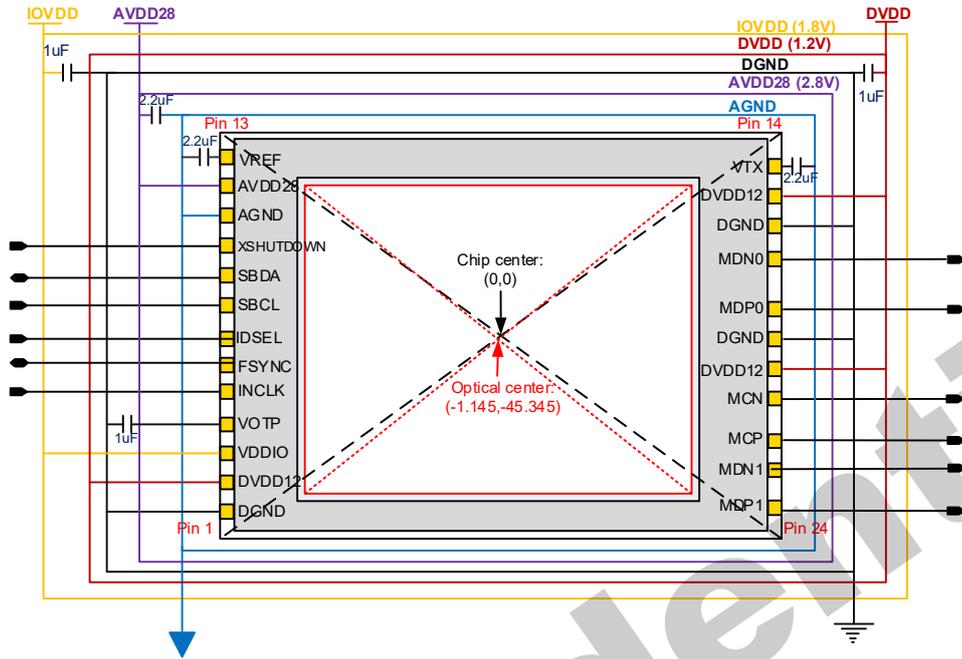
Figure 3-3 Peripheral Circuit Design

Note:

1. DGND & AGND should be maintained separated and connect to each other near the connector.

4. Optical Specifications

4.1 Readout Position

In default status, the first pixel to read out of GC05A2 is located at the lower left corner near pin 1. The image is inverted vertically and horizontally by the lens, which results in a mirrored image output. Readout direction can be set by register 0x0101[1:0].
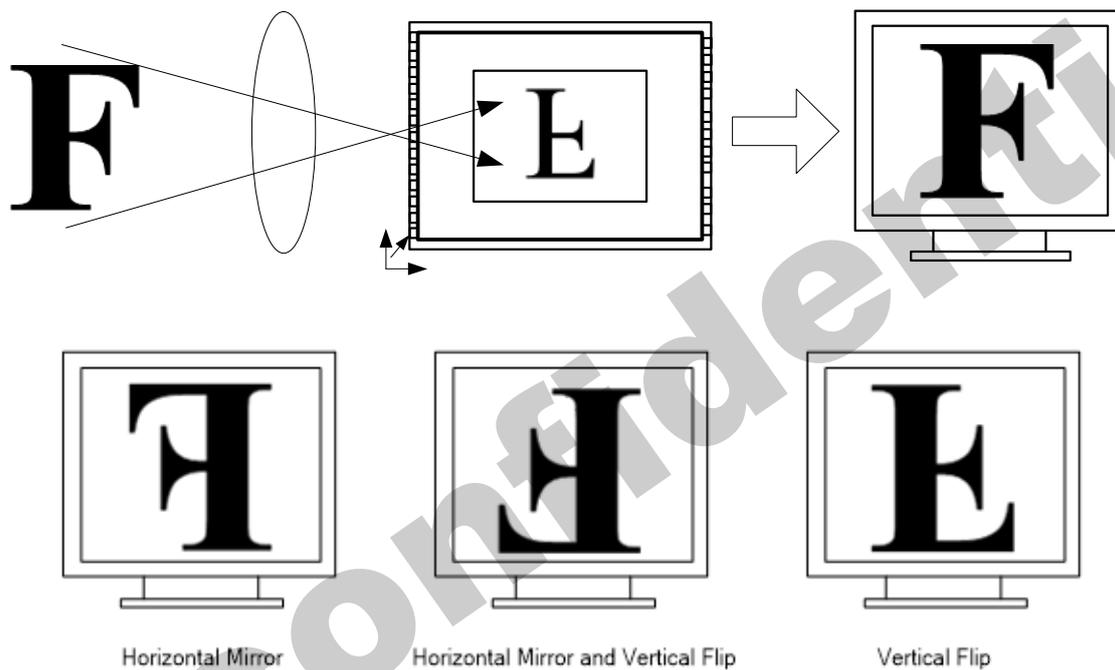
Figure 4-1 Readout Direction

Table 4-1 Mirror and Flip Information

Function	Register Address	Register Value	First Pixel
Normal	0x0101[1:0]	00	Gr
Horizontal mirror	0x0101[1:0]	01	R
Vertical Flip	0x0101[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0101[1:0]	11	Gb

Note:

1. GC05A2 supports auto first pixel selection, which means the actual output first pixel could be always maintained as Gr channel.

4.2 Pixel Array
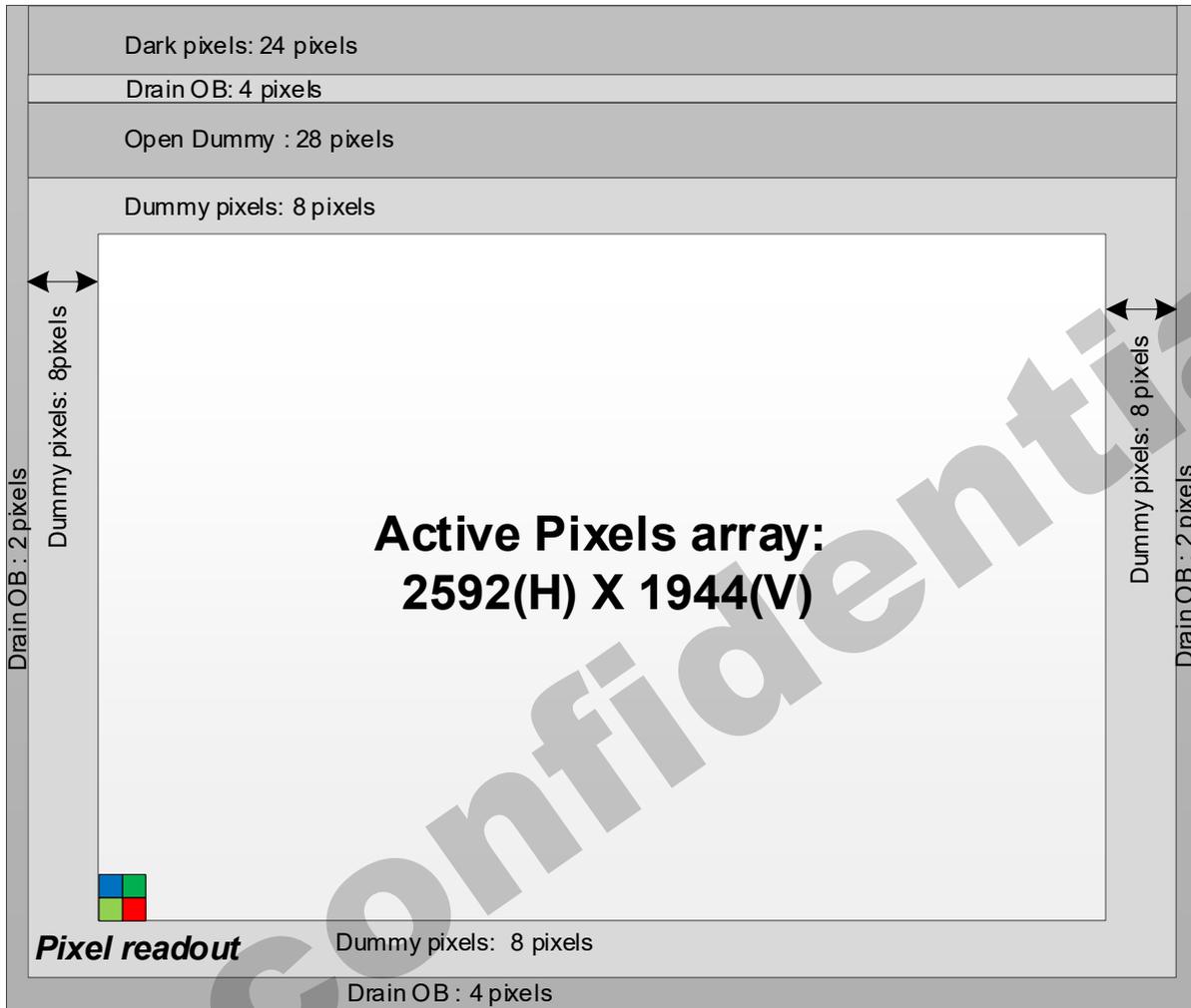
Figure 4-2 Pixel Array Information

4.3 Lens Chief Ray Angle (CRA)
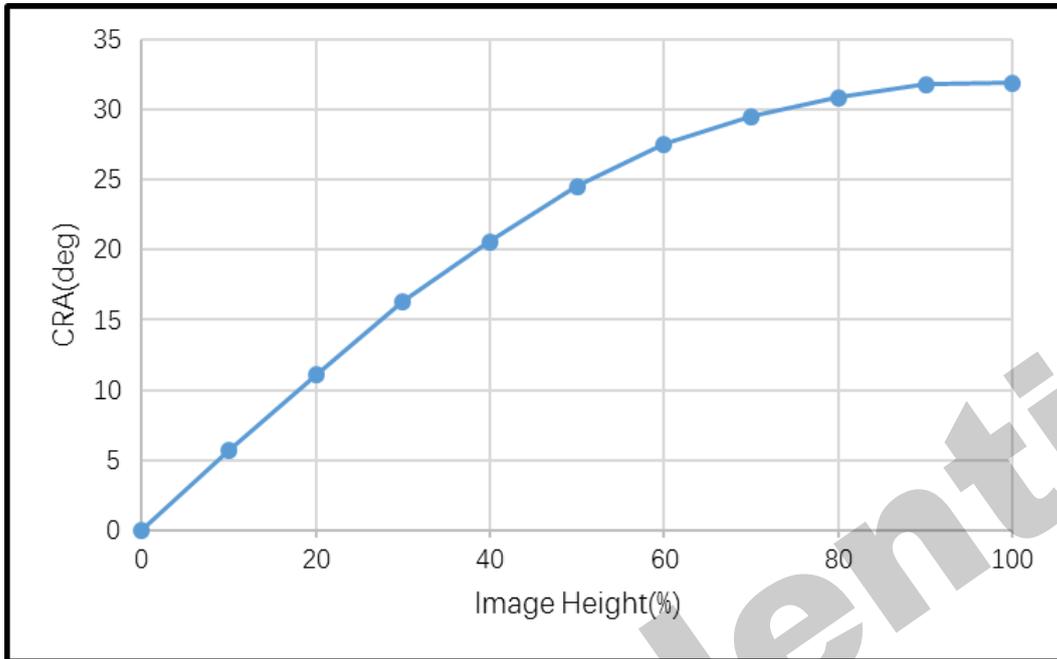
Figure 4-3 CRA Information

Table 4-2 CRA Information

Image Height (%)	Image Height (mm)	CRA (degree)
0	0.000	0.00
10	0.181	5.65
20	0.363	11.09
30	0.544	16.32
40	0.726	20.59
50	0.907	24.53
60	1.089	27.54
70	1.270	29.53
80	1.452	30.87
90	1.633	31.80
100	1.814	31.90

4.4　Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:
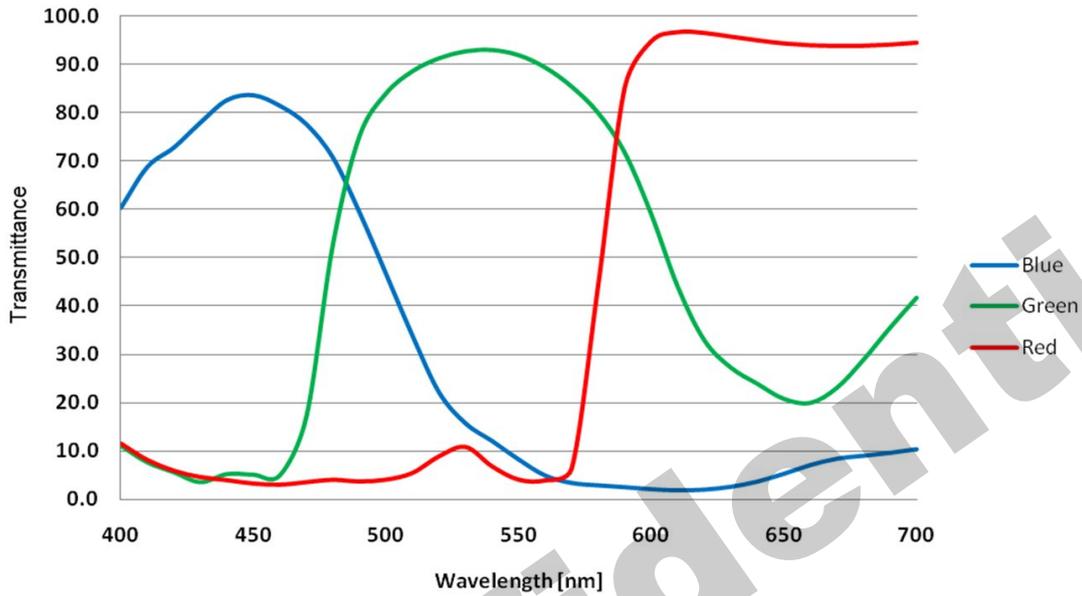
Figure 4-4 Color Filter Spectral Characteristics

5. Two-wire Serial Bus Communication

GC05A2 Device Address:

Table 5-1 Supported Device Address List

IDSEL PIN	Slave address write mode	Slave address read mode
L (default) **DGND**	**0x6e**	**0x6f**
H IOVDD	0x7e	0x7f

5.1 Protocol

The host must perform the role of a communication master and GC05A2 acts as either a slave receiver or transmitter. The master must do:

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL.**

There are two kinds of writing operation as well as two kinds of corresponding reading operation, as shown in the following figures.

(a) Writing operation (2 bytes address – 1 byte data)
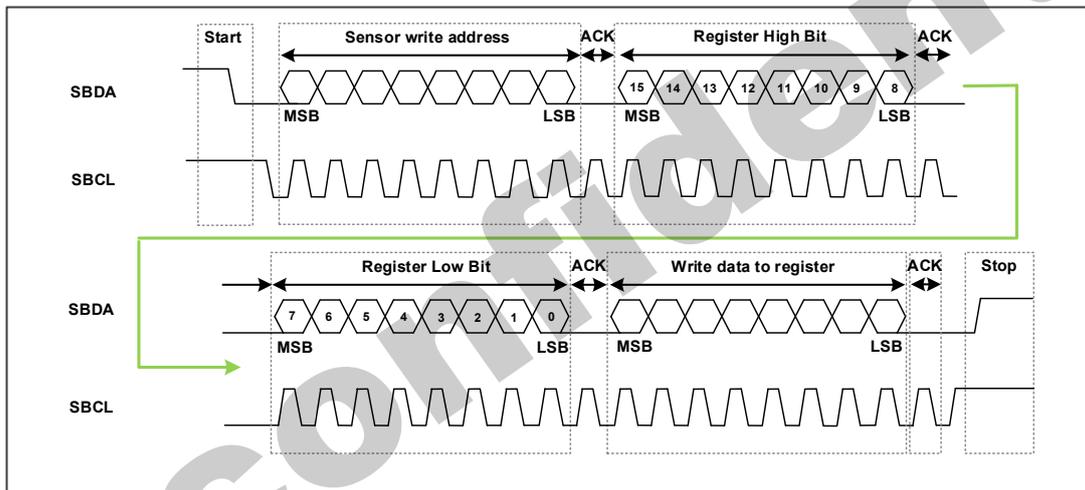
Figure 5-1 Writing Operation (2 bytes address – 1 byte data)

(b) Writing operation (2 bytes address – 2 bytes data)
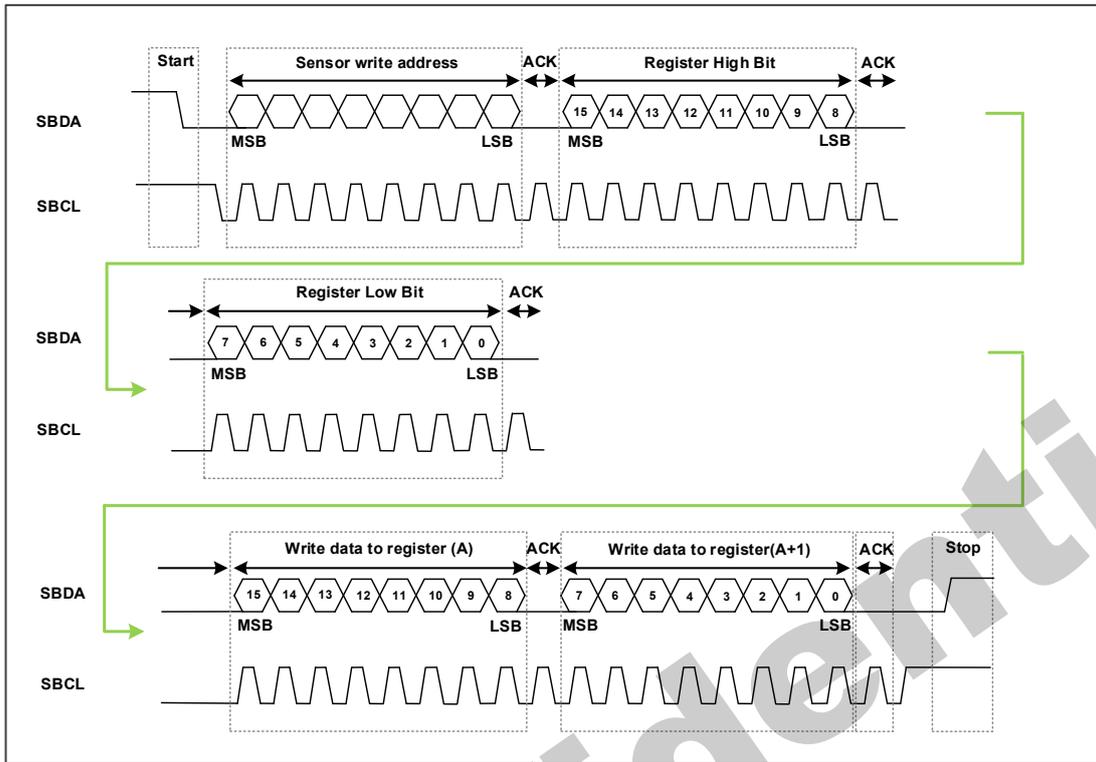
Figure 5-2 Writing Operation (2 bytes address – 2 bytes data)

(c) Reading Operation (2 bytes address – 1 byte data)
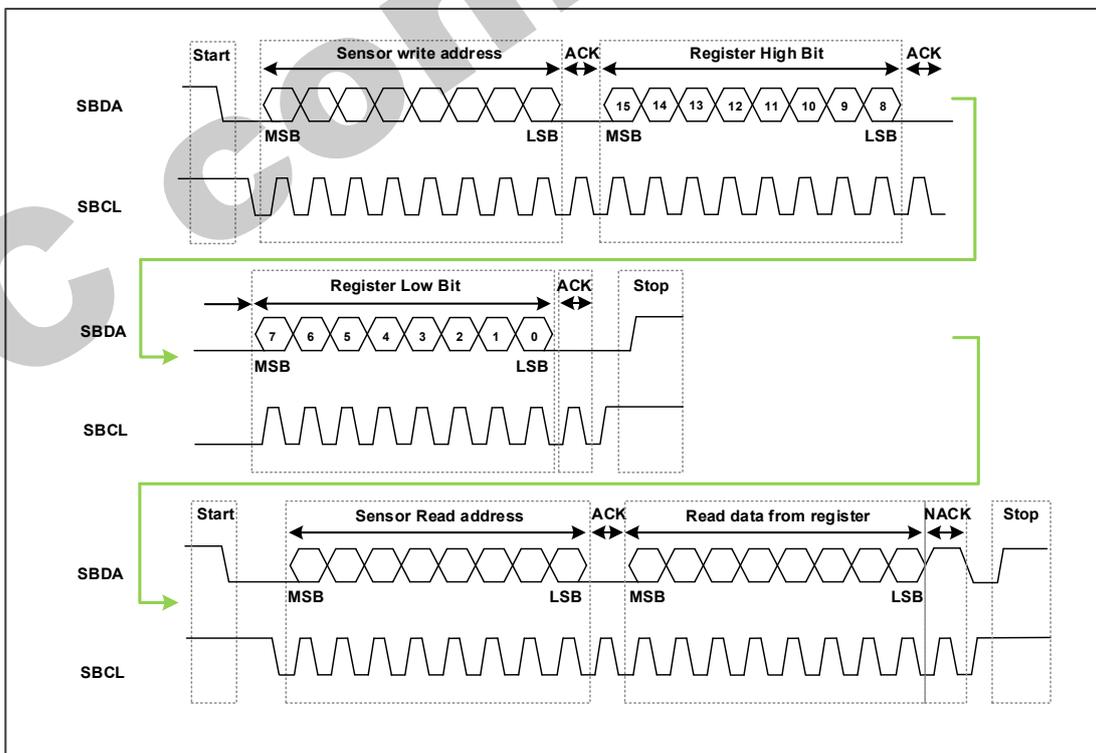
Figure 5-3 Reading Operation (2 bytes address – 1 byte data)

(d) Reading Operation (2 bytes address – 2 bytes data)
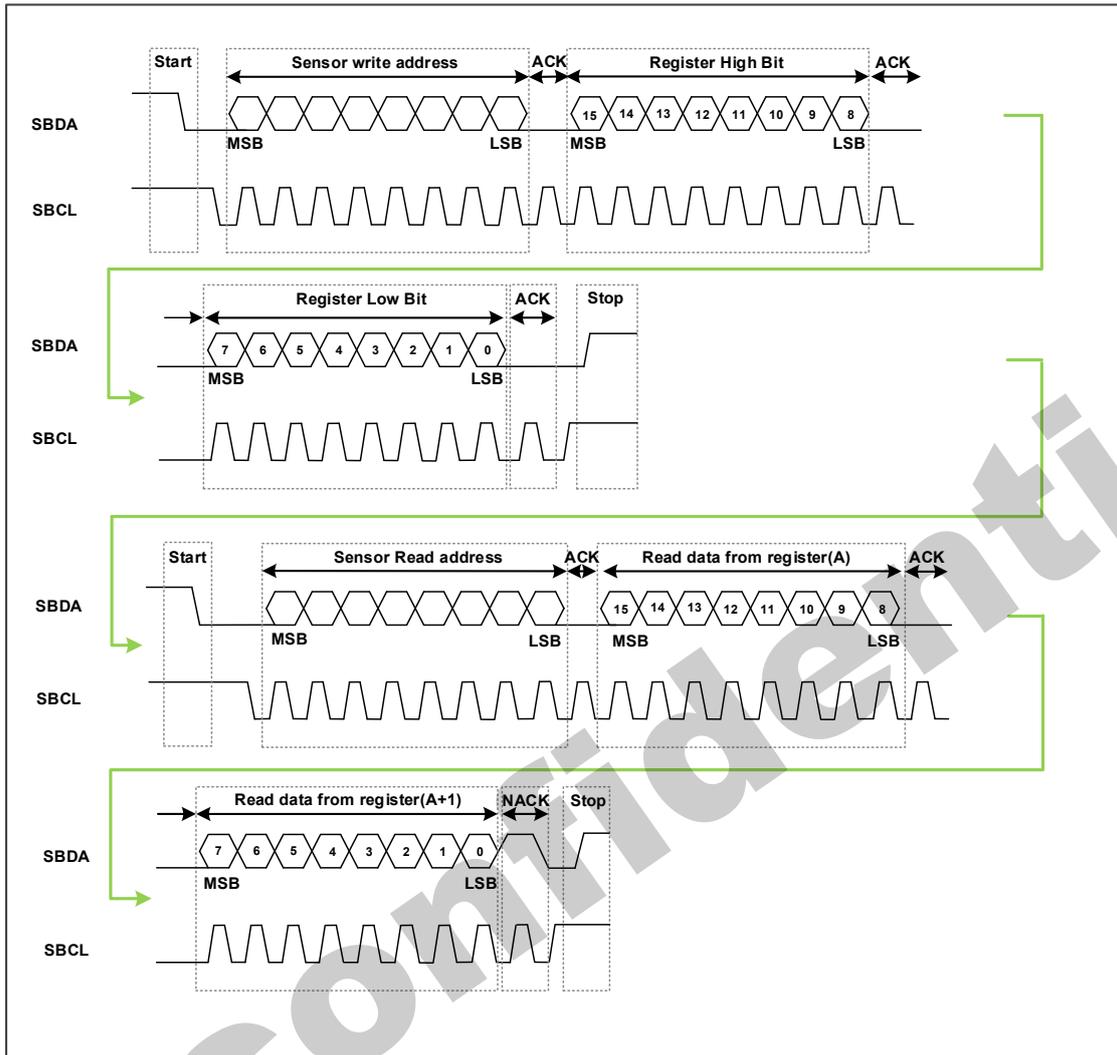
Figure 5-4 Reading Operation (2 bytes address – 2 bytes data)

5.2 Serial Bus Timing
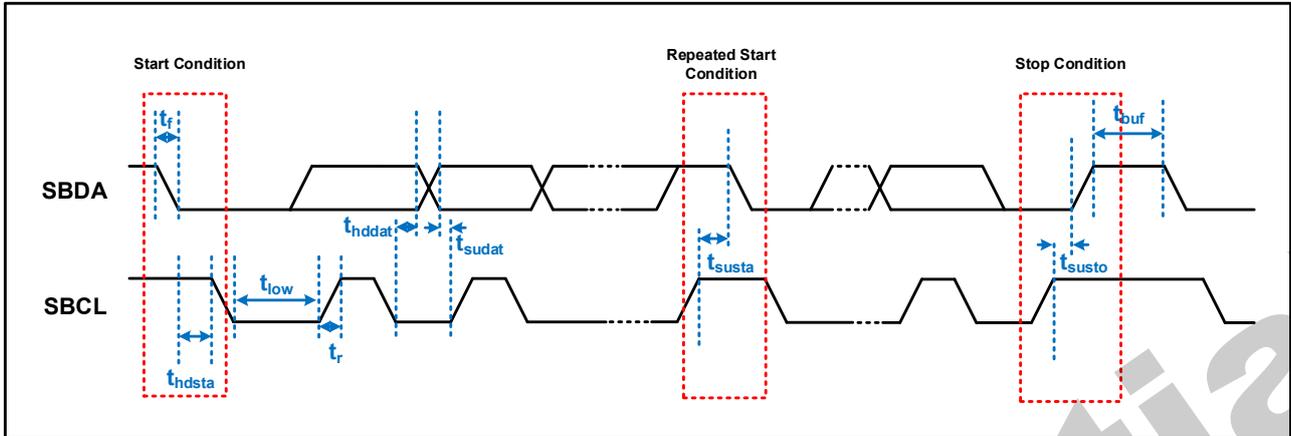
Figure 5-5 Serial Bus Timing Diagram

Table 5-2 Two-wire serial communication AC specification: Fast-mode

Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	µs
Hold time for start condition	$t_{hd;sta}$	0.6	--	--	µs
LOW period of SBCL	t_{low}	1.3	--	--	µs
HIGH period of SBCL	t_{high}	0.6	--	--	µs
Set-up time for repeated start condition	$t_{su;sta}$	0.6	--	--	µs
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for stop condition	$t_{su;sto}$	0.6	--	--	µs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	400	pf

Table 5-3 Two-wire serial communication AC specification: Fast-mode plus

Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	1000	KHz
Bus free time between stop and start condition	t_{buf}	0.5	--	--	μs
Hold time for start condition	$t_{hd;sta}$	0.26	--	--	μs
LOW period of SBCL	t_{low}	0.5	--	--	μs
HIGH period of SBCL	t_{high}	0.26	--	--	μs
Set-up time for repeated start condition	$t_{su;sta}$	0.26	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	50	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	120	ns
Fall time of SBCL, SBDA	t_f	--	--	120	ns
Set-up time for stop condition	$t_{su;sto}$	0.26	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	550	pf

Note:

1. Fast-mode plus supports only available with INCLK ≥ 16MHz.

6. MIPI Transmission

6.1 Clock Lane Low-Power
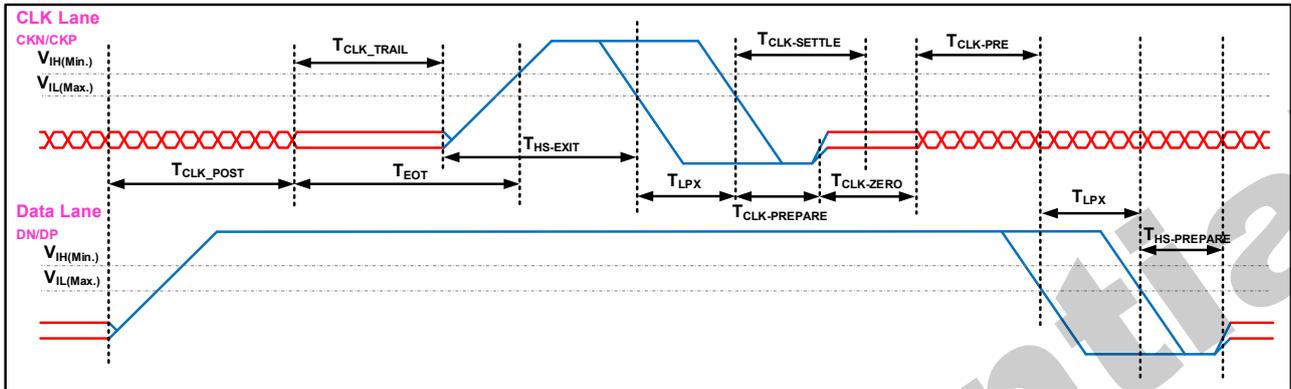
Figure 6-1 MIPI Clock Lane Diagram

Note:

1. Clock must be reliable during high speed transmission and mode-switching.

2. Clock can go to LP only when data lanes are in LP (and nothing relies on it).

3. In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

Table 6-1 shows some detailed register addresses for modifying the clock lane timing.

Table 6-1 Detailed Register Addresses for MIPI Clock Timing

Register Address	Description
0x0db4	$T_{CLK\_HS\_PREPARE}$
0x0db5	T_{CLK_ZERO}
0x0db6	T_{CLK_PRE}
0x0bd8	T_{CLK_POST}
0x0db9	T_{CLK_TRAIL}

6.2 HS Data Transmission
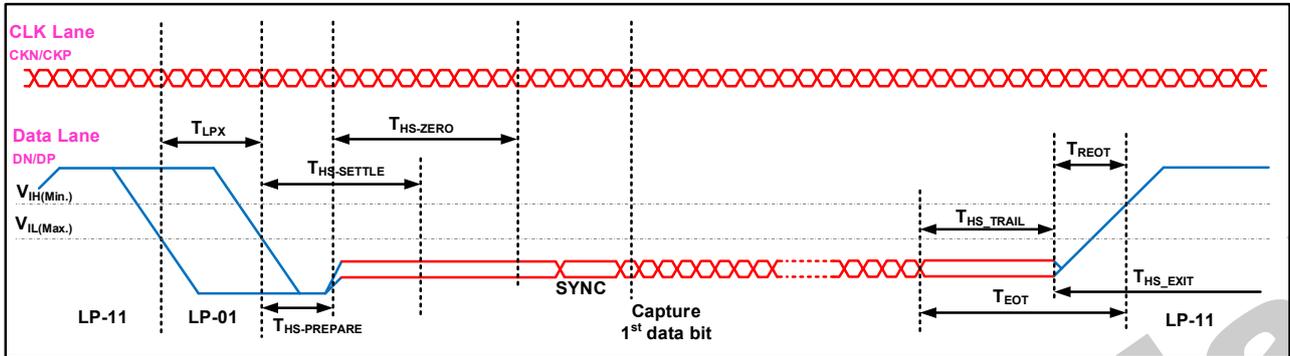
Figure 6-2 HS Data Transmission

Note:

1. Clock keeps running and samples data lanes (except for lanes in LPS).

2. Unambiguous leader and trailer sequences required to distill real bits.

3. Trailer is removed inside PHY (a few bytes).

4. Time-out to ignore line values during line state transition.

Table 6-2 shows some detailed register addresses for modifying the data lane timing.

Table 6-2 Detailed Register Addresses for MIPI Data Timing

Register Address	Description
0x0d93	T_{LPX}
0x0d94	$T_{HS\_PREPARE}$
0x0d95	T_{HS_ZERO}
0x0d99	T_{HS_TRAIL}
0x0d9b	T_{HS_EXIT}

7. Function Description

7.1 Operation mode

The GC05A2 supports three different operating states: Hardware Standby, Software standby, and streaming.

The transition between these states are achieved by issuing proper mode command via the CCI Serial control interface, XSHUTDOWN signal state, and power supplies. Figure 7-1 shows the transition between these states.
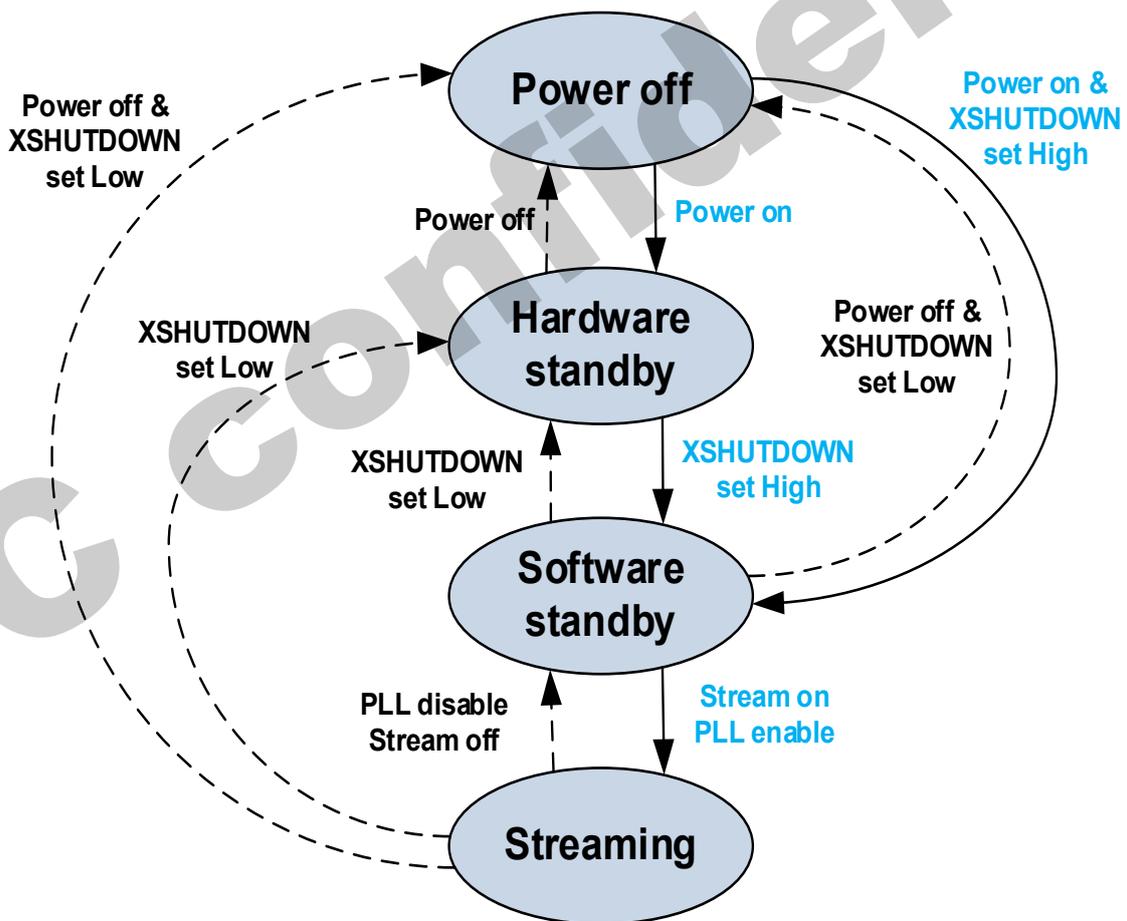
Figure 7-1 Operation Mode Switching Diagram

Table 7-1 Detailed Description of Different Operation Mode

Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN	XSHUTDOWN low
Software standby	Two- wire serial communication with sensor, PLL is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

7.2 Power on Sequence
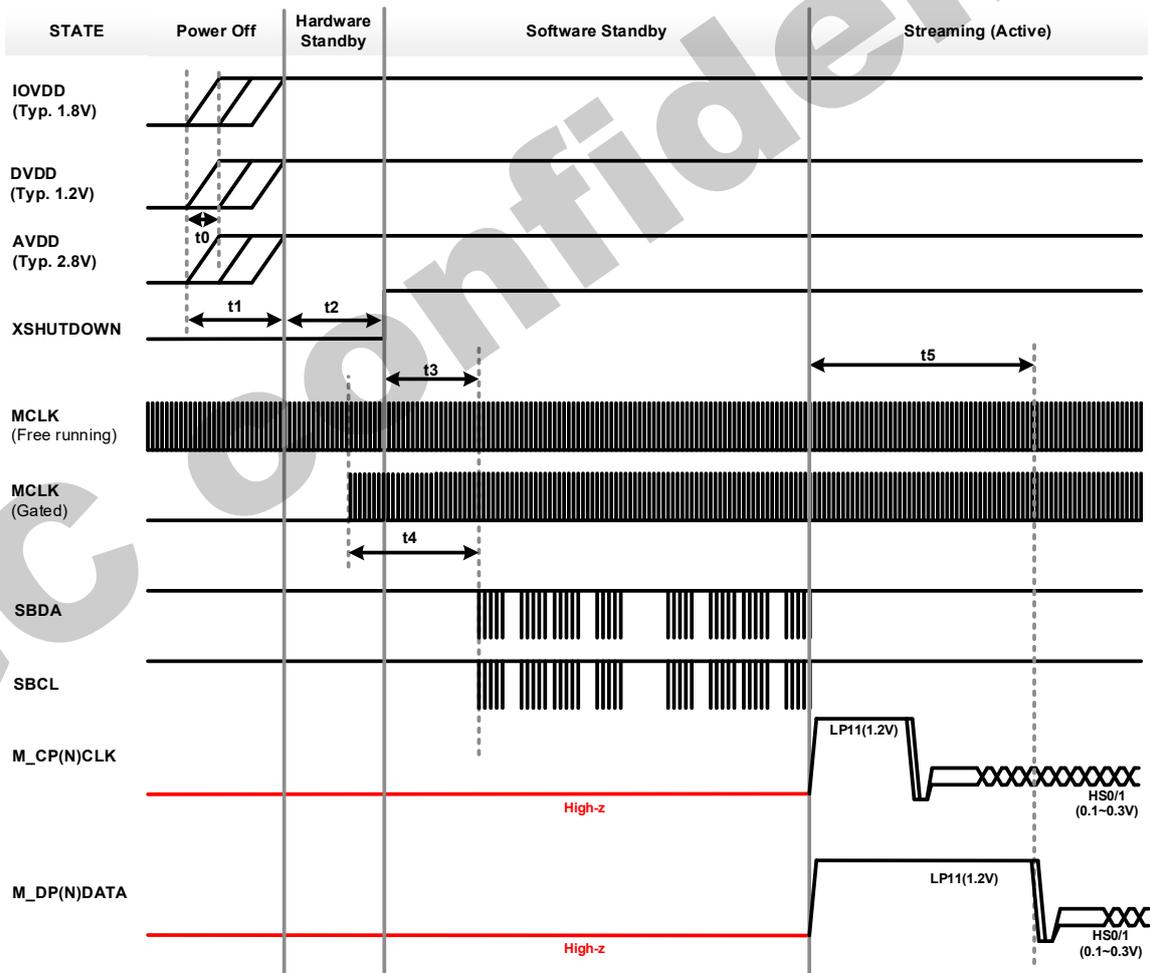
Figure 7-2 Power on Sequence

Table 7-2 Detailed Timing Description of Power on Sequence

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 rising time	50	-	µs
t1	IOVDD, DVDD12 and AVDD28 may rise in any order so the rising separation time can vary from 0µs to indefinite	0		µs
t2	From power on to XSHUTDOWN pull high	0	-	µs
t3	From XSHUTDOWN pull high to first I2C transaction	50	-	µs
t4	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t5	Entering streaming mode – First frame start sequence	Depend on the setting		ms

7.3 Power off Sequence
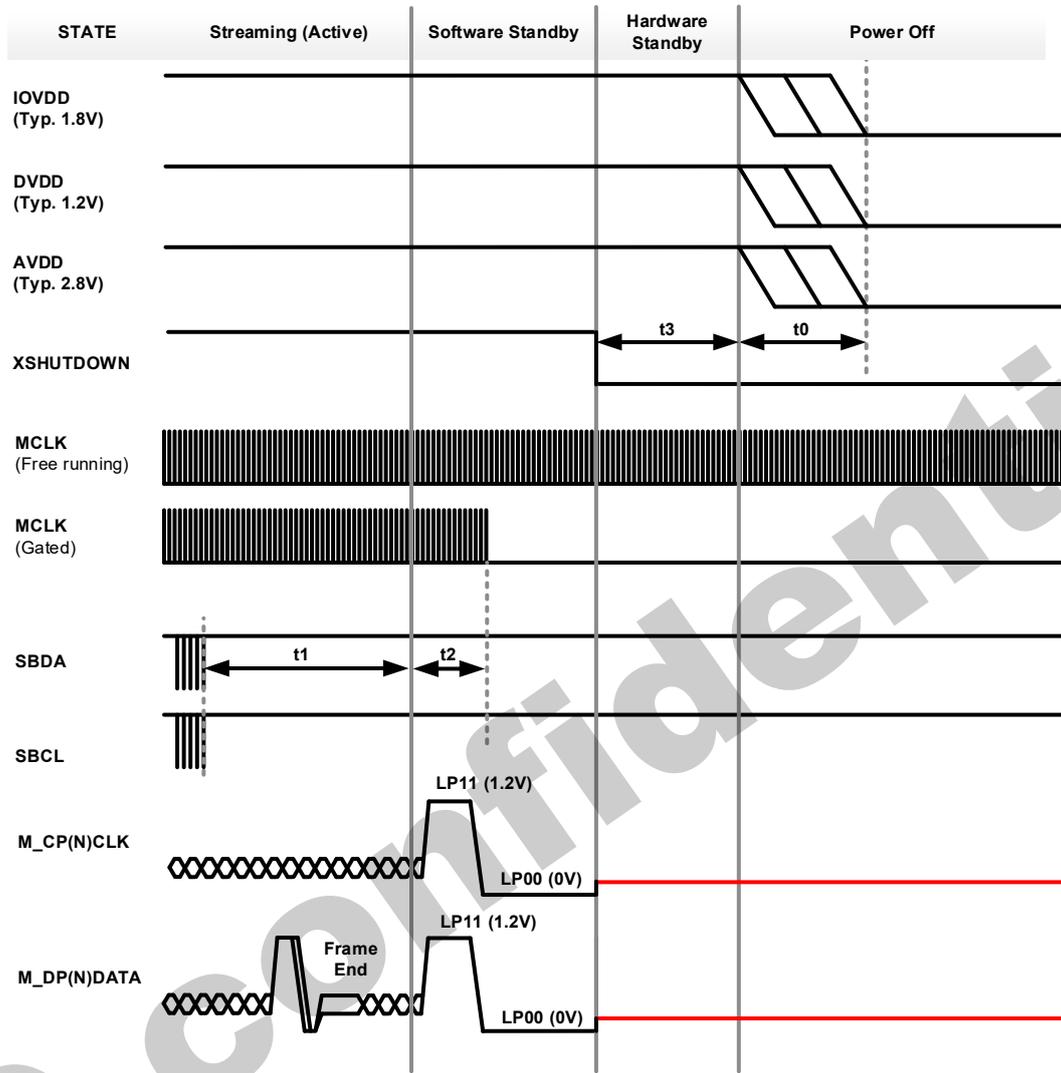
Figure 7-3 Power off Sequence

Table 7-3 Detailed Timing Description of Power off Sequence

Parameter	Description	Min.	Max.	Unit
t0	IOVDD, DVDD12 and AVDD28 may pull down in any order, so the falling separation time can vary from 0μs to indefinite	0	-	μs
t1	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t2	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK
t3	From XSHUTDOWN pull low to AVDD28/DVDD12 pull down	0	-	μs

Note:

1. If the sensor's power cannot be cut off, please keep power supply, then set XSHUTDOWN pin low. It will make sensor standby.

2. Registers should be reloaded before working.

3. If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

7.4 Black Level Calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

7.5 Integration Time

The integration time is controlled by the shutter time registers. When you want to set an exposure value that is bigger than the current frame length value, you should first set a new frame length and make sure that it's bigger than the exposure value you'd like to set.

Table 7-4 Integration Time Registers

Addr.	Register name	Description
0x0202	Shutter time	[6:0] shutter time[14:8]
0x0203		[7:0] shutter time[7:0]
0x0340	Frame length	[7:0] frame length[15:8]
0x0341		[7:0] frame length[7:0]

7.6 Gain Control

GC05A2 supports analog gain control through registers. The analog gain is controlled by total gain register with the precision of 6.10, which means 0x0400 represents 1x analog gain. The maximum supported analog gain is 16x. The detailed registers for analog are listed in table 7-5.

Table 7-5 detailed registers for analog gain and digital gain control

Address	Register name	Description
0x0204	Total gain	[7:0] total gain[15:8]
0x0205		[7:0] total gain[7:0]

7.7 Binning Mode

Binning read out mode can be used to obtain an image of lower resolution for full field of view, with lower output data rate. The following diagram describes on 2x2 averaged binning operations. Pixels of two adjacent rows and columns are averaged, and read out as one output pixel.
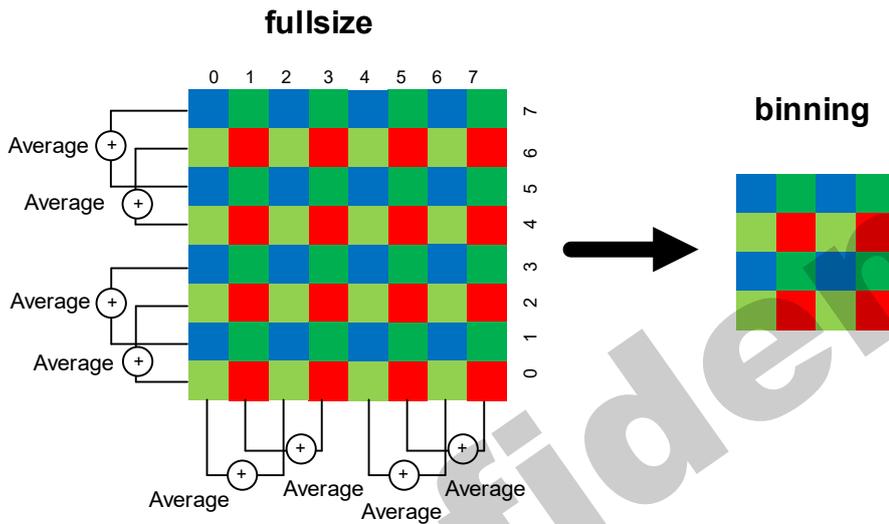
Figure 7-4 Binning Operation

7.8 Windowing

GC05A2 has a rectangular pixel array of 2592 x 1944, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.
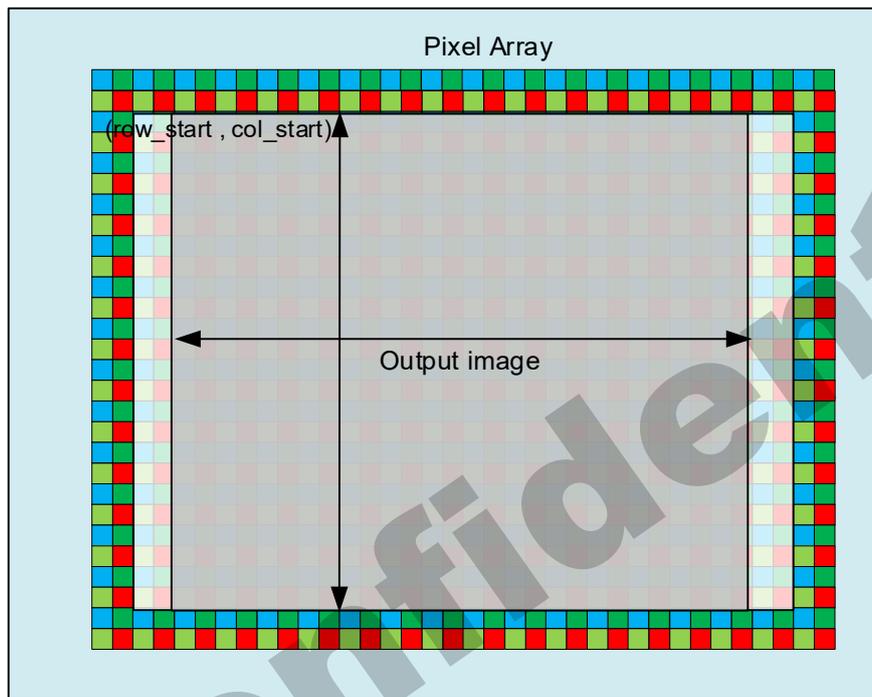
Figure 7-5 Windowing Control

Table 7-6 Detailed Registers for Windowing Control

Addr.	Register name	Description
0x0d14	Col start	[2:0]col_start[10:8]
0x0d13		[7:1]col_start[7:0]
0x0346	Row start	[2:0]row_start[10:8]
0x0347		[7:0]row_start [7:0]
0x00c0	win_width	[3:0]win_width[11:8]
0x00c1		[7:1]win_width[7:1]
0x034a	win_height	[2:0]win_height[10:8]
0x034b		[7:0]win_height[7:0]

Table 7-7 Out Window Set Register

Addr.	Register name	Description
0x0353	out_win_x1	[3:0] out_win_x1[11:8]
0x0354		[7:0] out_win_x1[7:0]
0x034c	out_win_width	[3:0] out_win_width[11:8]
0x034d		[7:0] out_win_width[7:0]

7.9 Dual Sync Application

GC05A2 supports VSYNC IN/OUT for dual sync master/slave application.
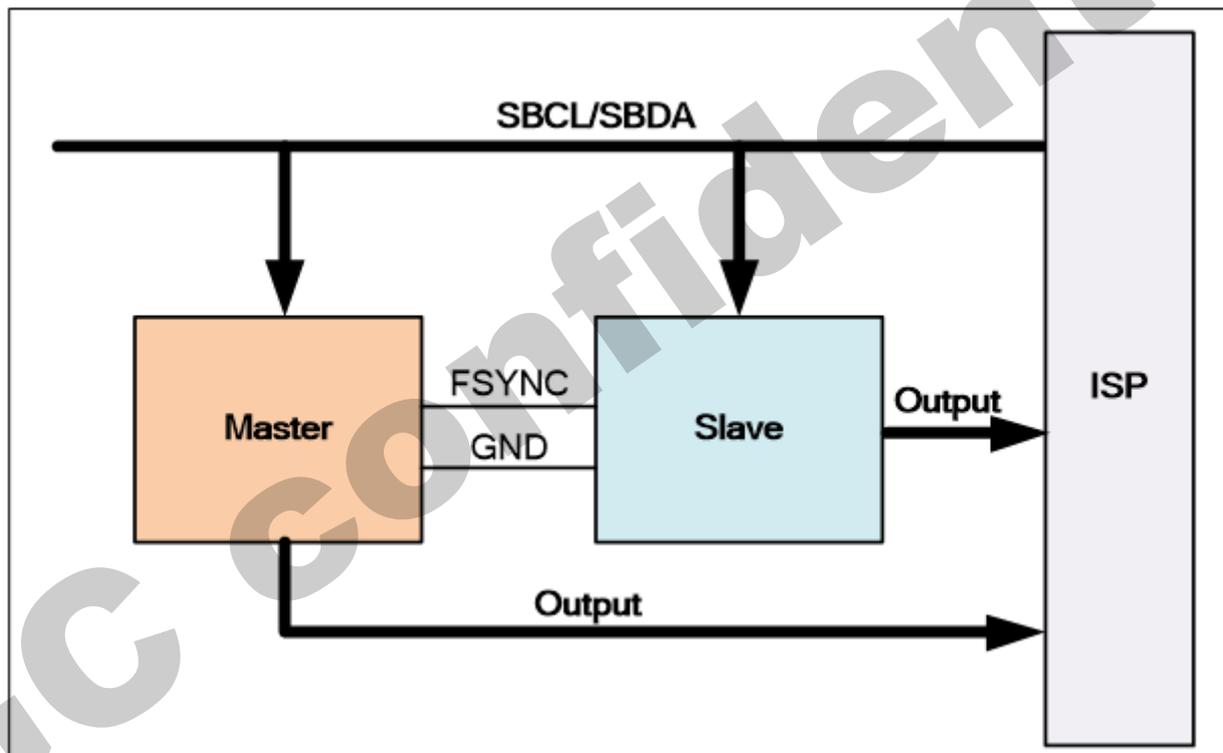
Figure 7-6 Dual Sync Application Configuration

When operating as slave, GC05A2 supports real-time synchronization. After receiving the frame sync signal from master, GC05A2 will firstly clear the row counter to make the frame header align with the master. However, this operation could lead to a corrupted frame so it's not recommended to start the synchronization operation while streaming. After the

alignment and the image data transmission, the slave will not transmit another frame of image data until it receives next frame sync signal from master. Figure 7-7 shows the detailed timing diagram of slave mode.

Note:

1. Both the FSYNC pin and GND pin of master and slave should be connected to each other for dual sync application.

2. Frame length should always be set shorter than master when doing AEC in slave mode.
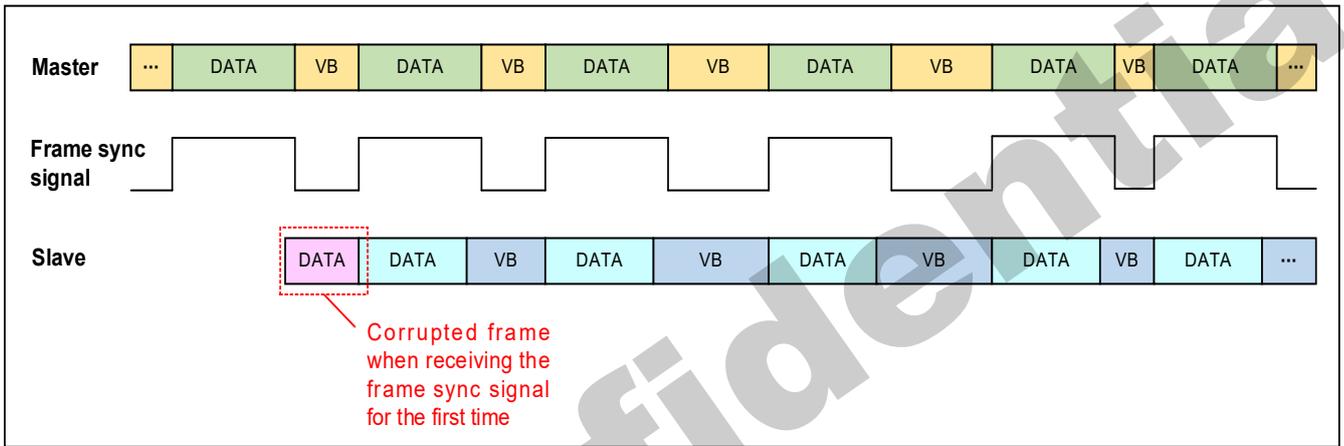
Figure 7-7 Dual Sync Mechanism

Table 7-8 Dual Sync Related Registers

Register Address	Bit (s)	Register Value		Description
		Slave	Master	
0x0237	[1]	1	0	Slave enable
	[0]	0	1	Master enable
0x0236	[4]	0	1	vsync_out_mode
0x0230	[2]	1	0	fine_Rowcnt_first_mode
	[1]	1	0	fine_Rowcnt_new_mode
	[0]	1	0	RowCnt mode
0x0230	[5]	1	1	Frame sync clock enable
	[4]	1	1	Frame sync function enable

7.10 Frame Structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length is controlled by window height, minimum VB and shutter time.

- Minimum frame length = min_FL(Reg[0x0220,x0221]) +32

- If shutter time(Reg[0x0202, 0x0203]) <= minimum frame length-16,

 Actual frame length = minimum frame length

- If shutter time > minimum frame length-16,

 Actual frame length = shutter time + 16. (recommended).

Line length control

Line length = 5862 (not recommended to be modified)

Table 7-9 Frame Structure Related Registers

Address	Register name	Description
0x0342	Line length	[5:0] Line length[13:8]
0x0343		[7:0] Line length[7:0]
0x0340	Frame length	[7:0] frame length[15:8]
0x0341		[7:0] frame length[7:0]

Note:

1. The actual line length should be three times of the value of line length register.

Blank time control

1. line blank time (HB) is controlled by line length

2. frame blank time (VB)

 - frame blank time = frame length– window height (Reg[0x034a, 0x034b])-16.
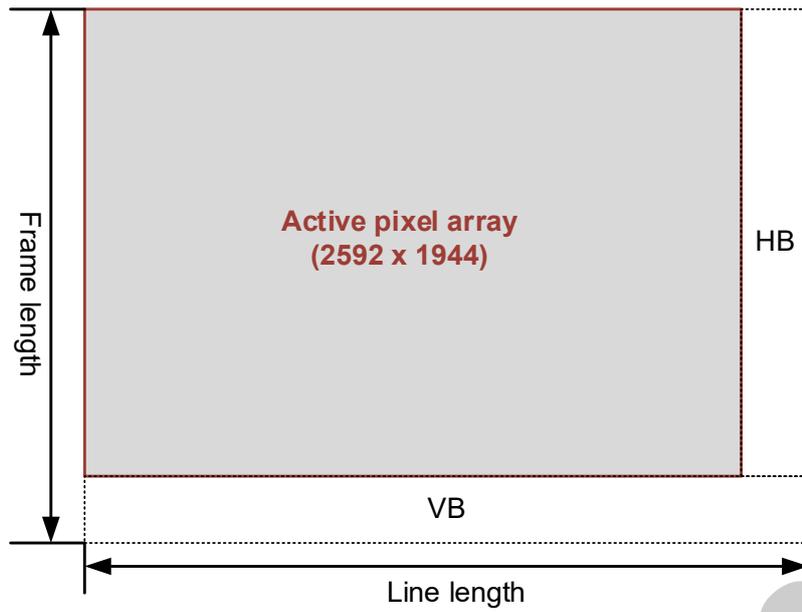
Figure 7-8 Frame Structure

7.11 OTP Memory

GC05A2 sensor has 64K bits embedded OTP (One Time Programmable) memory and 56K bits are for customers to store module calibration date, etc.

8. Register List

8.1 System Register

Address	Name	Default Value	R/W	Description
0x03f0	chip_ID_H	0x05	RO	[7:0] Sensor_ID
0x03f1	chip_ID_L	0xa2	RO	[7:0] Sensor_ID
0x0136	pllmp_div	0x38	RW	[7:0] pllmp_div
0x0202	Shutter time	0x00	RW	[6:0] shutter time[14:8]
0x0203		0x10	RW	[7:0] shutter time[7:0]
0x0340	frame_length	0x0c	RW	[7:0] frame length[15:8]
0x0341		0x60	RW	[7:0] frame length[7:0]
0x0342	line_length	0x08	RW	[5:0] Line length[13:8]
0x0343		0x00	RW	[7:0] Line length[7:0]
0x0d13	col_start	0x05	RW	[7:0] col_start[7:0]
0x0d14		0x00	RW	[2:0]col_start[10:8]
0x0346	row_start	0x00	RW	[2:0] row_start[10:8]
0x0347		0x04	RW	[7:0] row_start[7:0]
0x00c0	win_width[11:8]	0x0a	RW	[3:0]win_width[11:8]
0x00c1	win_width[7:0]	0x30	RW	[7:0] win_width[7:0]
0x034a	win_height	0x07	RW	[2:0] win_height[10:8]
0x034b	win_height	0xa8	RW	[7:0] win_height[7:0]
0x021c	long_exp[18:0]	0x00	RW	[2:0] long exp[18:16]
0x021d		0x00	RW	[7:0] long exp[15:8]
0x021e		0x00	RW	[7:0] long exp[7:0]

8.2 GAIN Control

Address	Name	Default Value	R/W	Description
0x0204	total_gain	0x04	RW	[7:0] total_gain [15:8]
0x0205		0x00	RW	[7:0] total_gain [7:0]
0x0090	WB_R_gain[11:0]	0x400	RW	[3:0] WB_R_gain[11:8]
0x0091				[7:0] WB_R_gain[7:0]
0x0092	WB_G_gain[11:0]	0x400	RW	[3:0] WB_G_gain[11:8]
0x0093				[7:0] WB_G_gain[7:0]
0x0094	WB_B_gain[11:0]	0x400	RW	[3:0] WB_B_gain[11:8]
0x0095				[7:0] WB_B_gain[7:0]

8.3 Out Window control

Address	Name	Default Value	R/W	Description
0x034c	out_win_width	0x0a	RW	[3:0] out_win_width[11:8]
0x034d		0x20	RW	[7:0] out_win_width[7:0]
0x0350	win_mode	0x01	RW	[0] win_mode
0x0353	out_win_x1	0x00	RW	[3:0] out_win_x1[11:8]
0x0354		0x00	RW	[7:0] out_win_x1[7:0]
0x005a	WB_offset	0x40	RW	[7:0] WB_offset

8.4 OTP

Address	Name	Default Value	R/W	Description
0x0a66	OTP	0x00	RW	[6] OTP_write (RO) [5] OTP_read (RO)
0x0a67	OTP_mode	0x00	RW	[7] OTP_en
0x0a69	OTP_access_addr	0x00	RW	[7:0] OTP_addr[15:8]
0x0a6a		0x00	RW	[7:0] OTP_addr[7:0]
0x0a6b	OTP_write_value	0x00	RW	[7:0] OTP_write_value
0x0a6c	OTP_read_value	-	R	[7:0] OTP_read_value

8.5 MIPI

Address	Name	Default Value	R/W	Description
0x0100	standby	0x00	RW	[0] standby
0x0101	Image_Orientation	0x00	RW	[1] updown [0] mirror
0x0117	MIPI	0x01	RW	[7] Lane_Ena_tmp [5] ULP_Ena_tmp [4] MIPI_enable_tmp
0x0d81	DPHY_mode	0x10	RW	[1:0] clk lane_mode
0x0dd2	LP_set_CLane	0x29	RW	[5:4] LP_NEW [3:2] LP_ONE [1:0] LP_ZERO
0x0dda	LP_set_DLane	0x29	RW	[7:6] LP_Z [5:4] LP_NEW [3:2] LP_ONE [1:0] LP_ZERO
0x0db1	T_init_set	0x80	WO	T_init_set
0x0db3	T_LPX_set	0x12	WO	T_LPX_set
0x0db4	T_CLK_HS_PREPARE_set	0x0d	WO	T_CLK_HS_PREPARE_set
0x0db5	T_CLK_zero_set	0x4b	WO	T_CLK_zero_set
0x0db6	T_CLK_PRE_set	0x02	WO	T_CLK_PRE_set
0x0db8	T_CLK_POST_set	0x16	WO	T_CLK_POST_set
0x0db9	T_CLK_TRAIL_set	0x0f	WO	T_CLK_TRAIL_set
0x0dbb	T_HS_exit_set	0x10	WO	T_HS_exit_set
0x0dbe	T_wakeup_set	0x80	WO	T_wakeup_set
0x0d94	T_HS_PREPARE_set	0x06	WO	T_HS_PREPARE_set
0x0d95	T_HS_Zero_set	0x0a	WO	T_HS_Zero_set
0x0d99	T_HS_TRAIL_set	0x08	WO	T_HS_TRAIL_set
0x0d9b	T_HS_exit_set	0x10	WO	T_HS_exit_set
0x0115	frame_counter	0x00	RW	[7:0] frame_counter[15:8]
0x0116		0x00	RW	[7:0] frame_counter[7:0]

Address	Name	Default Value	R/W	Description
0x0dd3	DPHY_analog_mode5	0x18	RW	[5:2] mipi_diff
0x0dd8	DPHY_Dlane0_mode	0x10	RW	[5:4] data0ctr [3] data0ph_en [2:0] data0lp_drv

8.6   ISP Related

Address	Name	Default Value	R/W	Description
0x0040	BLK_mode1	0x12	RW	[7:5] reserved [1] dark current enable [0] reserved
0x008c	Test image enable	0x00	RW	[0] test image enable
0x008d	Test image setting	0x10	RW	[7:4] test image mode 0000: solid_color 0001: color_bars 0010:fade_to_gray_color_bars 0011: PN9 0100: horizental_gradient 0101:checkerboard pattern 0110: slant 0111: resolution [3:0] solid_color_value
0x005a	WB_offset	0x40	RW	[7:0] WB_offset